CLAIMS

1. A circuit for biasing an input node of a sense amplifier, the circuit comprising:

means for keeping the input node at a pre-set operative voltage during a sensing operation;

means for pulling the input node from a starting voltage towards a power supply voltage, the operative voltage being comprised between the starting voltage and the power supply voltage; and

control means for disabling the means for pulling before the input node reaches the operative voltage.

2. The circuit according to claim 1, wherein the control means are connected in feedback to the input node for generating a completion signal when a voltage at the input node reaches a threshold value comprised between the starting voltage and the operative voltage, the means for pulling being disabled in response to the completion signal.

3. The circuit according to claim 1, wherein the means for keeping the input node at the operative voltage includes a voltage regulator including:

a cascode transistor having a control terminal, a first terminal and a second terminal, the first terminal being connected to the input node;

a feedback inverter connected between the input node and the control terminal of the cascode transistor; and

a current generator for supplying a biasing current to the feedback inverter, the biasing current being substantially independent of temperature and of the power supply voltage.

4. The circuit according to claim 3, wherein the voltage regulator further includes filtering means connected to the control terminal of the cascode transistor.

5. The circuit according to claim 4, wherein the filtering means includes a plurality of diodes and a resistor connected in series, each diode having a threshold voltage decreasing with the temperature and the resistor having a resistance increasing with the temperature.

6. The circuit according to claim 3, including further means for pulling the second terminal of the cascode transistor towards the power supply voltage, and still further means for pulling the control terminal of the cascode transistor towards the power supply voltage, the control means disabling the further means for pulling and the still further means for pulling before the input node reaches the operative voltage.

7. The circuit according to claim 6, wherein the control means includes a further feedback inverter having an input terminal connected to the input node and an output terminal providing the completion signal, the further feedback inverter having a threshold voltage lower than the operative voltage, and wherein each of the means for pulling, the further means for pulling and the still further means for pulling includes a corresponding pull-up transistor having a control terminal connected to the output terminal of the further feedback inverter.

8. A sense amplifier, comprising:

an input node; and

a circuit for biasing the input node, the circuit including:

means for keeping the input node at a pre-set operative voltage during a sensing operation;

means for pulling the input node from a starting voltage towards a power supply voltage, the operative voltage being comprised between the starting voltage and the power supply voltage; and

control means for disabling the means for pulling before the input node reaches the operative voltage.

9. The sense amplifier according to claim 8, further including an additional circuit, coupled with the circuit for biasing the input node, for receiving the completion signal.

10. A non-volatile memory device, comprising:

a plurality of memory cells; and

a sense amplifier for reading the memory cells, the sense amplifier, including:

an input node; and

a circuit for biasing the input node, the circuit including:

means for keeping the input node at a pre-set operative voltage during a sensing operation;

means for pulling the input node from a starting voltage towards a power supply voltage, the operative voltage being comprised between the starting voltage and the power supply voltage; and

control means for disabling the means for pulling before the input node reaches the operative voltage.

11. A method of biasing an input node of a sense amplifier, the method comprising the steps of:

keeping the input node at a pre-set operative voltage during a sensing operation; and

pulling the input node from a starting voltage towards a power supply voltage by use of corresponding means, the operative voltage being comprised between the starting voltage and the power supply voltage; and

disabling the means for pulling before the input node reaches the operative voltage.

12. A sense amplifier for reading a memory cell, the sense amplifier comprising:

a comparator; and

a regulator transistor connected between an input of the comparator and an array node connected to the memory cell, the regulator transistor having a control terminal, a first conduction terminal connected to the comparator input, and a second conduction terminal connected to the array node;

a first bias transistor connected between a supply voltage and the array node; and

a control element connected between the array node and a control terminal of the first bias transistor, and structured to turn off the first bias transistor in response to a voltage of the array node achieving a threshold voltage.

13. The sense amplifier of claim 12 wherein the control element includes a feedback inverter connected between the array node and the control terminal of the first bias transistor.

14. The sense amplifier of claim 13 wherein the regulator transistor is structured to maintain the array node at a predetermined operating voltage during reading of the memory cell and the feedback inverter has a threshold voltage that is less than the operating voltage such that the first bias transistor is turned off before the array node achieves the operating voltage.

15. The sense amplifier of claim 12, further comprising:

a feedback inverter connected between the array node and the control terminal of the regulator transistor.

16. The sense amplifier of claim 15, further comprising a current generator for supplying a biasing current to the feedback inverter, the biasing current being substantially independent of temperature and of the supply voltage.

17. The sense amplifier of claim 12, further including a clipper circuit connected between the control terminal of the regulator transistor and a reference voltage, the clipper circuit being structured to limit a voltage of the control terminal of the regulator transistor.

18. The sense amplifier of claim 17, wherein the clipper circuit includes a plurality of diodes and a resistor connected in series between the control terminal of the regulator transistor and the reference voltage, each diode having a threshold voltage decreasing with the temperature and the resistor having a resistance increasing with the temperature.

19. The sense amplifier of claim 12, further comprising a second bias transistor connected between the supply voltage and the first conduction terminal of the regulator transistor, the second bias transistor having a control terminal connected to

the control element which is structured to turn off the second bias transistor in response to the voltage of the array node achieving the threshold voltage.

20. The sense amplifier of claim 12, further comprising a second bias transistor connected between the supply voltage and the control terminal of the regulator transistor, the second bias transistor having a control terminal connected to the control element which is structured to turn off the second bias transistor in response to the voltage of the array node achieving the threshold voltage.